*IN THE SPECIFICATION*:

*Replace the paragraph beginning at page 1, line 4, with:*

The present invention relates to a multilayer-circuit semiconductor device having resistors and signal line region(s) and a method of fabricating the same. Particularly, this invention relates to the semiconductor device preventing relative fluctuations in resistance among the resistors and, moreover, preventing fluctuations in interconnection capacitance (stray capacitance) because of the influence of the interconnection patterns in upper or lower layers of the signal-wiring, and to a method of fabricating this semiconductor device.

*Replace the paragraph beginning at page 1, line 17, with:*

Conventionally, data performed between LSI's, such as memories, microcomputers, and logic elements to control electrical equipment and to perform video and audio signal processing. However, eRAM (embedded RAM) obtained by integrating these LSI's into one chip, based on progress in both process and design technologies, has been intensively focused on as a new device (i.e., system LSI). The eRAM obtained by integrating ASIC's, microcomputers, and large-capacity memories can realize equipment that is more compact, has higher-speed data transfer due to expanded bus width, and has lower power consumption as compared to a combination of a general-purpose memory and a microcomputer.

*Replace the paragraph beginning at page 2, line 4, with:*

As semiconductor devices are becoming still more highly integrated, the structure of the semiconductor device is becoming more and more complicated. The number of layers of a multilayer-circuit for a logic system have increased. Because of such complicated structure, the disadvantages described below have occurred. Specifically, depending on whether an interconnection pattern is present on upper or lower layers of a layer on which resistors ("resistor group") or signal line region(s) are provided, there may occur problems, such as thermal influence over these groups and regions due to sintering

during fabrication of the semiconductor, influences caused by fluctuations in stray capacitance due to a difference of thicknesses of the layers, and electrical influence during operation of the semiconductor. Accordingly, it becomes more important whether the resistor group and the signal line region located in a logic region can be operated stably.

*Replace the paragraph beginning at page 2, line 21, with:*

Fig. 6A is a plan view of DRAM consolidated logic that has been conventionally used. This DRAM consolidated logic has a DRAM region E1 and a logic region E2. Fig. 13 and Fig. 14 show cross-sectional views taking along line XIII-XIII of Fig. 6A showing a structure covering a first Al interconnection layer of the DRAM consolidated logic in Fig. 6A. In this type of DRAM-logic hybrid device, a cylindrical stacked capacitor (concave) having a certain height is formed in the DRAM region E1. The stacked capacitor is composed of a lower capacitor electrode layer 122, dielectric film 123, and an upper capacitor electrode layer 124.

*Replace the paragraph beginning at page 3, line 7, with:*

Fig. 13 shows an example of the DRAM consolidated logic including a region having the resistor group composed of a group of diffused resistors in the logic region E2. The resistor group arranged in the logic region E2 is provided to be used as additional resistors. In Fig. 13, the resistor group is composed of the belt-like isolation oxide films 105 spaced apart from and extending in parallel with each other on the main surface of the semiconductor substrate, and $N^+$ diffused regions 104 each extending between the belt-like isolation oxide films 105. The first Al interconnection layer 129 is located on the upper layer of the resistor group in the logic region E2.

*Replace the paragraph beginning at page 3, line 19, with:*

Fig. 14 shows an example of the DRAM consolidated logic including a region having the signal interconnection in the logic region E2. In Fig. 14, two different layers of signal interconnections are located in the logic region E2, that is, a signal interconnection 126a formed by utilizing a layer common to a bit line 126 in the DRAM region E1, and a signal interconnection 108a formed by utilizing a layer common to a gate electrode in the DRAM region E1. The first Al interconnection layer 129 is located above the region having the signal interconnections 108a and 126a.

*Replace the paragraph beginning at page 4, line 4, with:*

In the conventional art, however, in association with an increase in the number of interconnection layers in the logic region E2, the resistor group and the signal interconnection in the logic region E2 are affected by how a pattern is arranged on the upper layer or the lower layer. Therefore, the problems as follows occur.

*Replace the paragraph beginning at page 4, line 10, with:*

Firstly, there is a problem that relative resistance within the resistor group fluctuates depending on whether a pattern is present on the first Al interconnection layer 129 as the upper layer. For example, when any faults on a substrate produced due to etching or the like during fabrication are to be removed by sintering executed after formation of the first Al interconnection, removal of the faults on the substrate may become non-uniform due to presence or absence of a pattern on the first Al interconnection layer 129 as the upper layer. Traps caused by a boundary potential on the surface of the resistors may become non-uniform within the resistor group. Therefore, fluctuations in the relative resistance within the resistor group in an analog line or the like become a problem (see Fig. 13)